



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,413	01/26/2005	Hiroji Aga	121797	5555
25944	7590	10/04/2006		EXAMINER
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			JEFFERSON, QUOVAUNDA	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/522,413	AGA ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 26 January 2006.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-8 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>04/21/05</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities. Appropriate correction is required.

Claim 1 fails to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. For example, instead of "an insulating film formation step forming an insulating film on a first main surface of at least either one of a first substrate, and a second substrate composed of silicon single crystal" in lines 2-4 of claim 1, a more appropriate phrasing is "an insulating film formation step of forming an insulating film on a first main surface of at least either one of a first substrate and a second substrate composed of silicon single crystal".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al, US Patent 6,191,007.

Regarding claim 1, Matsui teaches a method of fabricating an SOI wafer comprising of an insulating film formation step forming an insulating film **2** on a first main surface of at least either one of a first substrate and a second substrate **1** composed of silicon single crystal (column 11, line 66 and column 12, line 2), a separatory ion implanted layer formation step, forming a separatory ion implanted layer **7** by implanting ions from the ion implantation surface on the first main surface side of the second substrate (figure 2a), a bonding step bonding the second substrate having the separatory ion implanted layer formed therein and the first substrate **8** while opposing the first main surfaces with each other, placing the insulating film in between (figure 2b), a separation step succeeding the bonding step, separating a bonded silicon single crystal film, later becoming an SOI layer, from the second substrate at the position of separatory ion implanted layer (figure 2c), and a planarization step planarizing the separation surface side of the bonded silicon single crystal film so as to produce the SOI layer (figure 2d), wherein, in the separatory ion implanted layer formation step, depth of formation of the separatory ion implanted layer measured from the ion implantation surface is adjusted through a magnitude of the ion implantation energy in order to adjust thickness of the bonded silicon single crystal film depending on thickness of the SOI layer to be obtained (column 12, lines 49-63).

Matsui fails to teach the dose of the ion implantation is set smaller as the depth of formation of the separatory ion implanted layer measured from the ion implantation surface becomes smaller. However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions, such as dose of the ion implantation, because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears *prima facie* that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claim 2, Matsui further teaches the planarization step further comprises a polishing step polishing the separation surface side of the bonded silicon single crystal film (Figure 2D and column 14, lines 45-48).

Regarding claim 3, Matsui fails to teach in the polishing step, polishing stock removal of the separation surface side of the bonded silicon single crystal film is set smaller as surface roughness of the separation surface of the bonded silicon single crystal film becomes smaller. However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions, such as desired surface smoothness, because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears *prima facie* that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claim 4, Matsui fails to teach the dose of the ion implantation is set smaller, and the polishing stock removal, in the polishing step, of the separation surface side of the bonded silicon single crystal film is set smaller, as the thickness of the SOI layer to be obtained becomes smaller. However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable

by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears *prima facie* that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claims 5-8, Matsui further teaches the insulating film is a silicon oxide film (column 12, line 5).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,245,645, issued to Mitani et al, discloses a method for fabricating an SOI layer. UK Patent Application, GB 2,211,911A, issued to United Kingdom Atomic Energy Authority, discloses electrical isolation of regions within

Art Unit: 2823

semiconductor bodies. US Patent 5,494,835, issued to Bruel, discloses process for the production of a relief structure on a semiconductor material support.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 10/522,413

Art Unit: 2823

Page 8



Fernando Toledo

Patent Examiner

Art Unit 2823

QVJ
QVJ.